(9) CLAIMS

1. A common-mode feedback circuit for a fully-differential operational amplifier device, the circuit comprising:

a first power supply input terminal for connecting to a first voltage potential;

a second power supply input terminal for connecting to a second voltage potential;

a first input terminal for connecting to a non-inverting output of said fully-differential operational amplifier device;

a second input terminal for connecting to an inverting output of said fully-differential operational amplifier device;

an output terminal for providing a common-mode feedback voltage;

bridging said first power supply terminal Vdd and said second power supply input terminal, first means for establishing a substantially constant bias current;

connected to said first means, to said first input terminal and said second input terminal, and to said second power supply input terminal, second means for changing division of said substantially constant bias current when signals to said first input terminal and said second input terminal are not in equilibrium;

bridging said first power supply input terminal and said second power supply input terminal and connected to said first means and said second means, third means for setting common-mode feedback voltage level at said output terminal, and

wherein said bias current is shared between said second means and said third means such that when inverting output and non-inverting output of said fully-differential operational amplifier device are not in equilibrium said bias current through said third means is changed via said second means wherein said third means provides said common-mode feedback reference voltage at a level for re-balancing said fully-differential operational amplifier device.

2. The circuit as set forth in claim 1 wherein said first means comprises:

a first MOSFET and a second MOSFET, wherein

respective source regions are connected to said first power supply input terminal,

respective gate regions are connected to a drain region of said first MOSFET,

said first MOSFET drain region is connected to a bias current supply, and

said second MOSFET drain region is connected to said second means.

3. The circuit as set forth in claim 2 wherein said second means comprises:

a third MOSFET having a gate region connected to said first input terminal, a source region connected to said drain region of said second MOSFET, and a drain

region connected to said second power supply input terminal, and a fourth MOSFET having a gate region connected to said second input terminal, a source region connected to said drain region of said second MOSFET, and a drain region connected to said second power supply input terminal, and

wherein respective body regions of said third MOSFET and said fourth MOSFET are connected to said first power supply input terminal.

4. The circuit as set forth in claim 3 wherein said third means comprises:

a fifth MOSFET having a source region connected to said third MOSFET source region and to said fourth MOSFET source region, a gate region and a drain region co-connected, and a body region connected to said first power supply input terminal, and

a sixth MOSFET having a source region and body region connected to said second power supply input terminal, a drain region and a gate region co-connected to said co-connected gate region and drain region of said fifth MOSFET, and said sixth MOSFET gate region is connected to said output terminal.

5. A multistage operational amplifier, comprising:

at least one fully-differential operational amplifier stage; and,

bridging outputs of each said fully-differential operational amplifier stage, a common-mode feedback device including first means for providing a substantially

constant current and second means, having a common-source connected input configuration, for dividing said current and for generating a feedback voltage to said fully-differential operational amplifier dependent upon division of said current therethrough such that feedback voltage is at a first level when inputs to said fully-differential operational amplifier are in equilibrium and at a second level for balancing said fully-differential operational amplifier when inputs to said fully-differential operational amplifier are not in equilibrium.

6. The invention as set forth in claim 5 wherein said first means further comprises:

a diode-connected MOSFET connected to a mirror MOSFET connected to a third MOSFET and a fourth MOSFET having said common-source connected input configuration.

7. The invention as set forth in claim 6 wherein said second means further comprises:

a MOSFET output stage generating said feedback voltage to said fully-differential operational amplifier dependent upon division of said current therethrough from said third MOSFET and said fourth MOSFET such that said feedback voltage is at said first level when inputs to said fully-differential operational amplifier are in equilibrium and at said second level for balancing said fully-

differential operational amplifier when inputs to said fully-differential operational amplifier are not in equilibrium.

8. The invention as set forth in claim 7 wherein said MOSFET output stage further comprises:

a series connected fifth MOSFET and sixth MOSFET wherein said fifth MOSFET is source-connected to said fourth MOSFET and outputs of said fully-differential operational amplifier and said sixth MOSFET provides said feedback voltage at said first level when inputs to said fully-differential operational amplifier are in equilibrium and at said second level for balancing said fully-differential operational amplifier when inputs to said fully-differential operational amplifier are not in equilibrium.

9. A common-mode feedback circuit device for a fully-differential operational amplifier, the circuit comprising:

a first MOSFET configuration for maintaining a substantially constant current to an output thereof; and

connected to said output and to respective outputs of said fully-differential operational amplifier, a second MOSFET configuration for dividing said current and driving a third MOSFET configuration connected thereto, wherein said third MOSFET configuration is generating a feedback voltage to said fully-differential

operational amplifier dependent upon division of said current therethrough such that feedback voltage is at a first level when inputs to said fully-differential operational amplifier are in equilibrium and at a second level for balancing said fully-differential operational amplifier when inputs to said fully-differential operational amplifier are not in equilibrium.

10. The device as set forth in claim 9, said fully-differential operational amplifier having a non-inverting output and an inverting output, said device further comprising:

a first power supply input terminal for connecting to a first power supply voltage level;

a second power supply input terminal for connecting to a second power supply voltage level;

a first input terminal for connecting to said non-inverting output of said fully-differential operational amplifier device;

a second input terminal for connecting to said inverting output of said fully-differential operational amplifier device;

an output terminal for providing a common-mode feedback voltage;

a first MOSFET and a second MOSFET, wherein respective source regions are connected to said first power supply input terminal, respective gate regions are connected to a drain region of said first MOSFET, said first MOSFET has a drain

region connected to a bias current supply, and said second MOSFET has a drain region connected to said second means;

a third MOSFET having a gate region connected to said first input terminal, a source region connected to said drain region of said second MOSFET, and a drain region connected to said second power supply input terminal;

a fourth MOSFET having a gate region connected to said second input terminal, a source region connected to said drain region of said second MOSFET, and a drain region connected to said second power supply input terminal; and

wherein respective body regions of said third MOSFET and said fourth MOSFET are connected to said first power supply input terminal;

a fifth MOSFET having a source region connected to said third MOSFET source region and to said fourth MOSFET source region, a gate region and a drain region co-connected, and a body region connected to said first power supply input terminal; and

a sixth MOSFET having a source region and body region connected to said second power supply input terminal, a drain region and a gate region co-connected to said co-connected gate region and drain region of said fifth MOSFET, and said sixth MOSFET gate region is connected to said output terminal.